Chips JU and RISC V – vision, actions, challenges.

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EUROPEAN PARTNERSHIP

Outline

1. What is Chips Joint Undertaking?
2. Evolution of the ECS JUs - Chips JU's predecessors.
3. Processor Design Ambition and Why RISC V in Europe.
4. Chips JU's support to RISC V.
5. Remaining Challenges.
6. Synergies with other activities.
7. Conclusions.

WHAT IS CHIPS JOINT UNDERTAKING?

Joint undertaking (JU)

A Joint Undertaking is an institutionalized **Public-Private Partnership** (**PPP**) with its **own legal identity**, with its own governance, budget etc.. The JUs are established by an EU regulation.

Chips JU

Chips JU was established in September, 2023, in an amendment to the Single Basic Act to implement the **first pillar of the Chips Act** and to continue the activities of its predecessors in the field of electronic components and systems (**ECS**). The Chips JU is a **tri-partite partnership** between the **EC**, the **participating states** and **European industries**; most of our actions are **funded jointly and equally** by these actors.

3IA - Chips JU private industrial members:

Aeneas

EPoSS. European Association on Smart Systems Integration

Inside Industry Association

The European Chips Act

European Semiconductor Board (Governance)

Pillar 1

Chips for Europe Initiative

- Initiative on infrastructure building in synergy with the EU's research programmes
- Support to start-ups and SMEs

Pillar 2

Security of Supply

- First-of-a-kind semiconductor production facilities

Pillar 3

Monitoring and Crisis Response

- Monitoring and alerting
- Crisis coordination mechanism with MS
- Strong Commission powers in times of crisis

Chips Act: Entry into force, 21 September 2023

Signatures 13 September, Publication 18 September 2023

Roberta Metsola (European Parliament President)

José Manuel Albares Bueno (Council Presidency)

Chips Act:

https://eur-lex.europa.eu/eli/reg/2023/1781/oj

Single Basic Act amendment:

https://eur-lex.europa.eu/eli/reg/2023/1782/oj

CHIPS JU AND ITS PREDECESSORS

First Generation JUs 2008-2014(FP7) – ENIAC and **ARTEMIS JU**

- full **bottom-up**
- first of its kind **tripartite model**

Second Generation JU 2014-2021 (H2020) – ECSEL JU

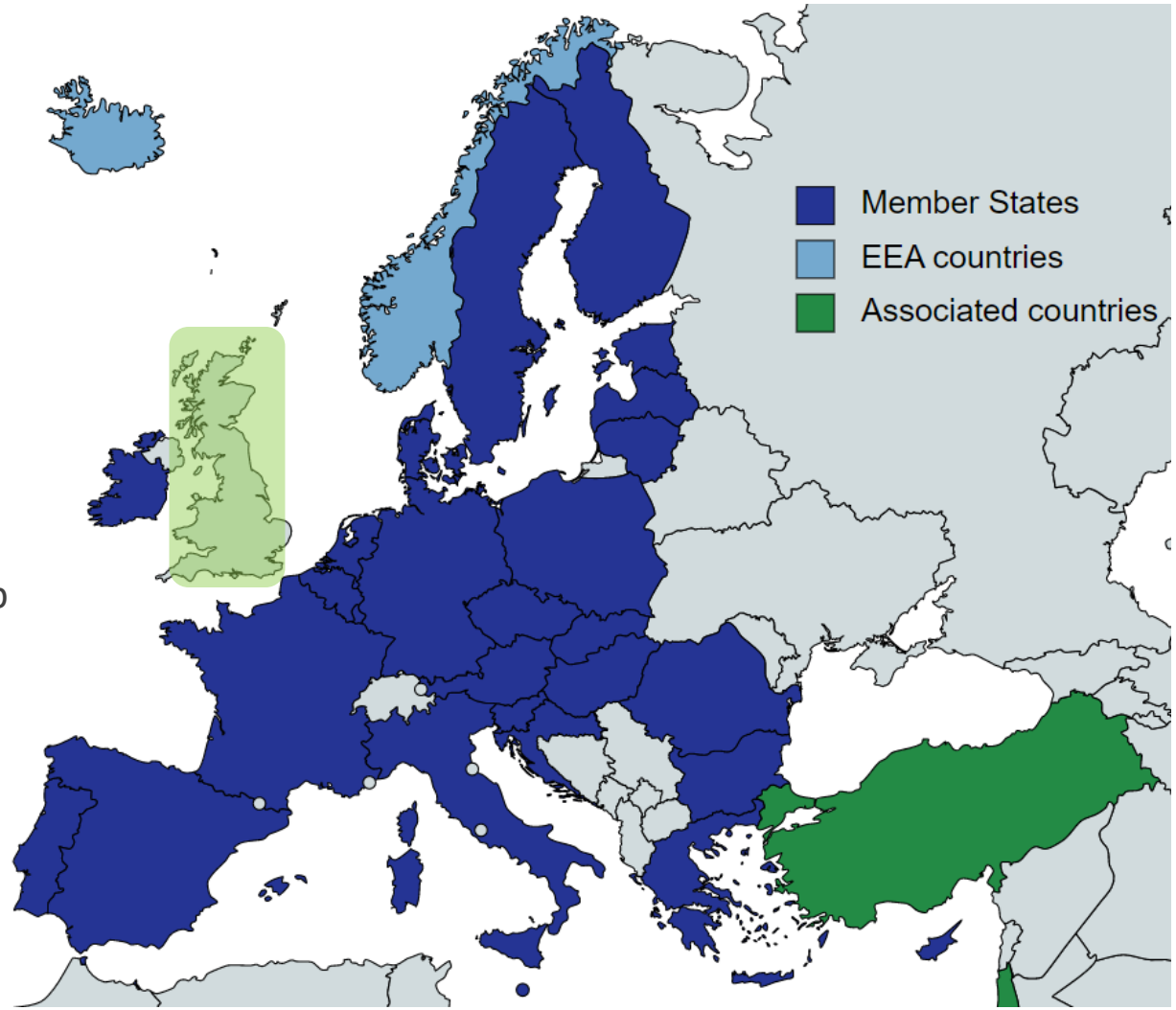
- full bottom-up **with some special topics**
- **lighthouse initiatives**: Mobile.E, Industry4.E, Health.E

Third Generation JUs 2021-2027 (HE)

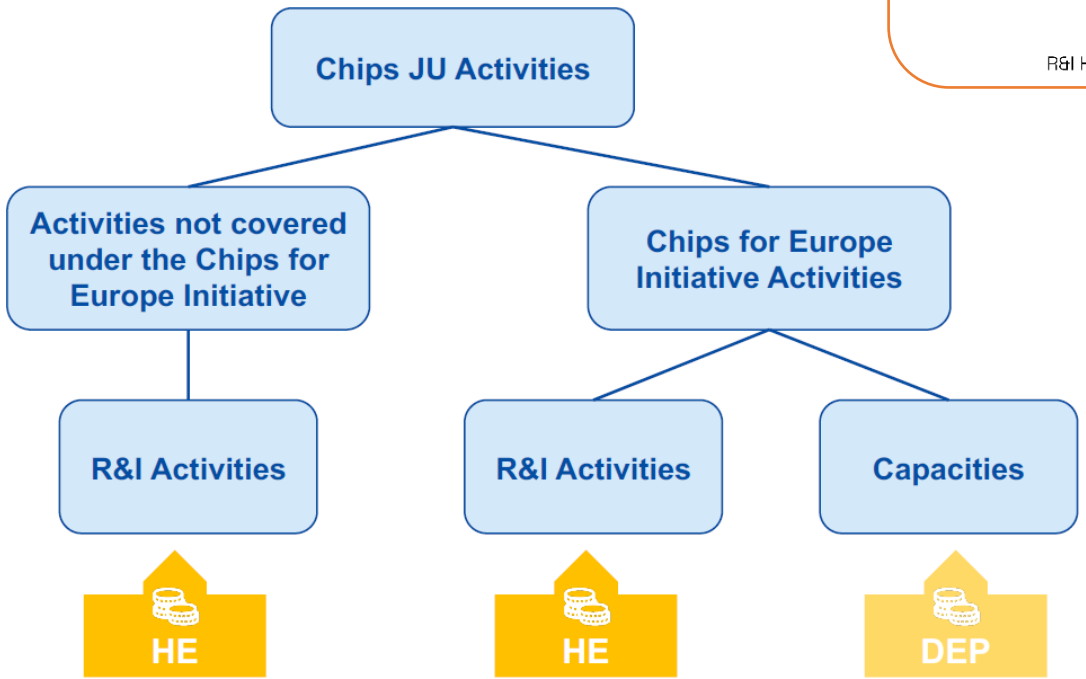
- **KDT JU (2021-2023) General Objectives**
  a) Reinforce **EU strategic autonomy** in electronic components and systems
  b) Establish **EU scientific excellence and innovation** leadership
  c) Ensure that components and systems technologies address **Europe's societal and environmental challenges**
- **From KDT to Chips JU (2023-2027)**
  d) Pilot lines
  e) Design platform
  f) Competence centers
  g) Quantum chips technology
  Digital Europe Programme in addition to **Horizon Europe**

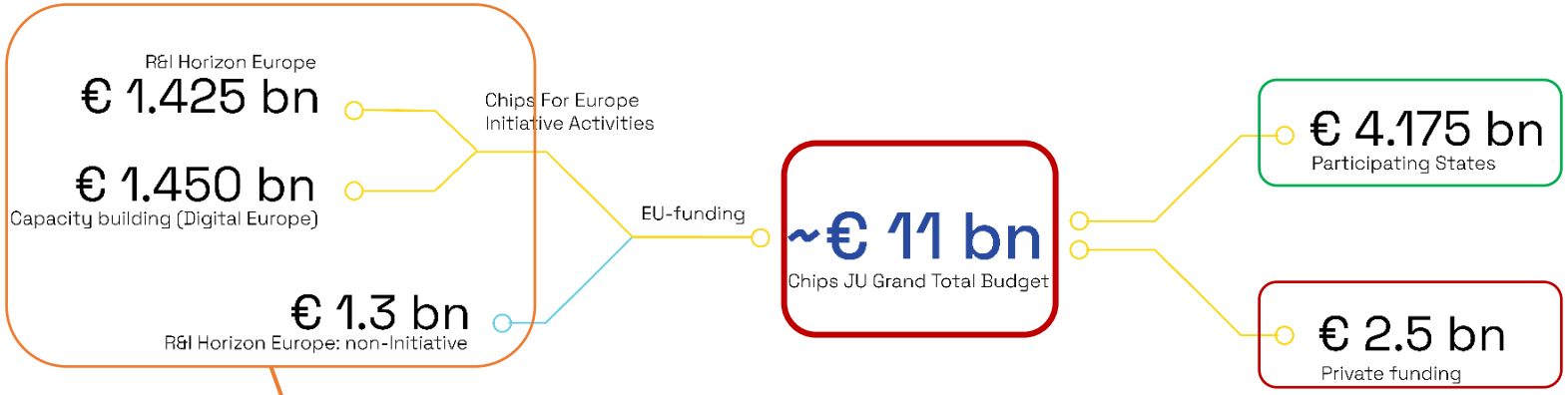
Non-initiative

Initiative



CHIPS JU – BUDGET STRUCTURE





EU Contribution to Chips JU (excl	Chips for Europe Initiative	Non-Initiative	Total
R&I (Horizon Europe)	€ 1.425 bn	€ 1.300 bn	€ 2.725 bn
Cap building (DEP)	€ 1.450 bn	n.a.	€ 1.450 bn
Total	**€ 2.875 bn**	**€ 1.300 bn**	**€ 4.175 bn**

CHIPS JU'S AMBITION FOR EUROPEAN PROCESSOR DESIGN

- Support the development of a **balanced portfolio of processor** families in the EU for the needs of various European industries.
- Approach processor design **holistically** - both at **HW** and **SW** levels.
- Cover the entire **value chain** from **SW applications to silicon**.
- Act in **cooperation** with other EU programmes to leverage R&I results.
- Secure **European technological sovereignty** and **reliability** in processor **supply chains.**

What Processor Architecture would serve the above ambitions efficiently?

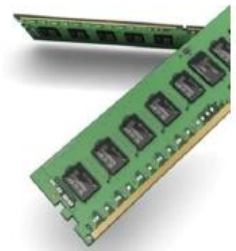
Why RISC V in Europe?

Recommendations and Roadmap for European Sovereignty in Open Source Hardware, Software, and RISC-V Technologies

Report from the

Open Source Hardware & Software Working Group

August 2022



Members of the Open Source HW/SW Working Group

- *Chair :*
  - Patrick Pype — NXP Semiconductors
- *Participants :*
  - Jan Andersson — Cobham Gaisler
  - Luca Benini — ETH Zürich / Univ. Bologna
  - Sven Beyer — Siemens
  - Holger Blasum — SYSGO GmbH
  - Sylvain Depierre — NanoXplore
  - Marc Duranton — CEA
  - Wolfgang Ecker — Infineon
  - Michael Gielda — Antmicro Ltd
  - Edwin Hakkennes — Technolution
  - Andreas Koch — Technische Universität Darmstadt
  - Loic Lietar — GreenWaves Technologies
  - Andreas Mauderer — Bosch
  - Jan-Hendrik Oetjens — Bosch
  - Jérôme Quévremont — Thales
  - John Round — NXP Semiconductors
  - Javier Serrano — CERN
  - Herbert Taucher — Siemens
  - Jean-Marc Talbot — Siemens
- EC Representatives
  - Georgi Kuzmanov — KDT JU
  - Panos Tsarchopoulos — DG CONNECT
  - Arian Swegers — DG CONNECT
- Editor
  - Haydn Thompson — THHINK

WHY RISC-V IN EUROPE – THE ECS COMMUNITY'S VIEW

SWOT by the Open Source HW/SW Working Group

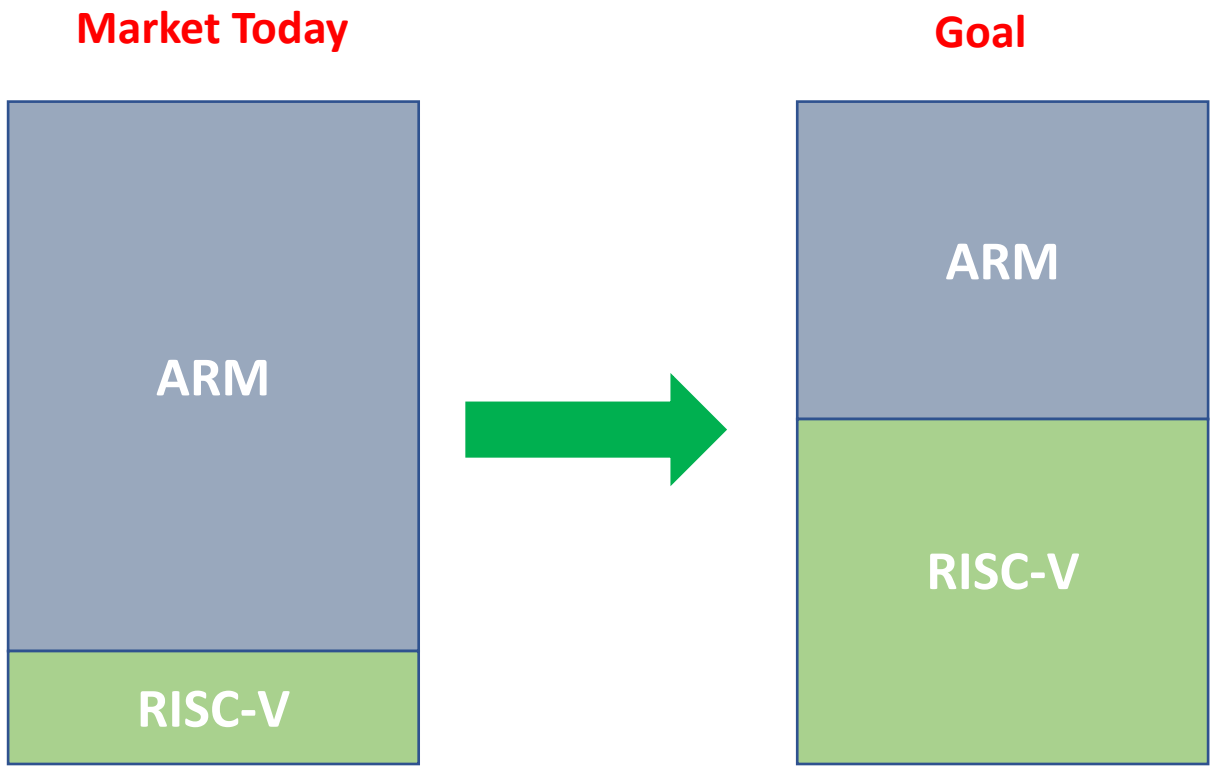
STRENGTHS - Easy access & low barrier for SoC design - Ability to customize - Accessible data for safety & security analysis (whitebox) - Availability of SW ecosystem - Lower export control restrictions - Less vulnerable to geo-political risks - Strong academic support ; educational use - Steers Innovation	***WEAKNESSES*** - Not Industrial Quality IP yet (HW/SW) - Long-term guaranteed support to industrial users not yet established - Risk of maintenance - Lack of some IP (e.g. interconnect)
OPPORTUNITIES - Customization opportunities - Sharing development costs - Sharing support costs - New licensing models - Support to SME's - New industrial leaders	***THREATS*** - Risk not to create enough critical mass in Europe - US/China competitors are running fast, with large investments and acceptance by leading end-user companies

Europe must develop the RISC-V supply chain to support autonomy in critical market sectors and reduce its dependency on US & China

MAXIMISE **RESOLVE**

Courtesy: Open Source HW/SW Working Group

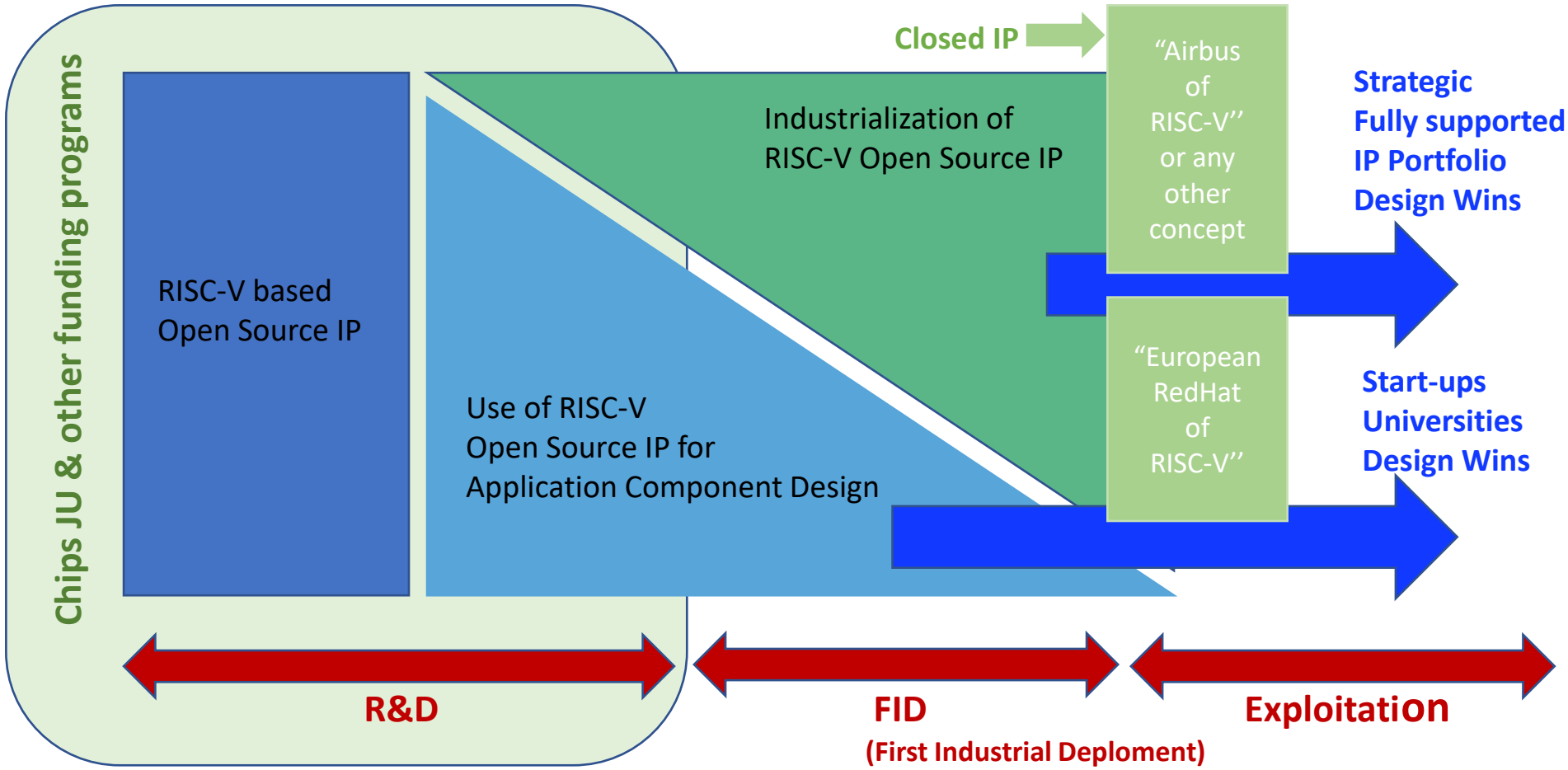
Need for a Balanced Portfolio



Provide a viable alternative on the market of Processor Cores

Courtesy: Open Source HW/SW Working Group

Approach to European Success Story



Courtesy: Open Source HW/SW Working Group

Chips JU’s Support to RISC V

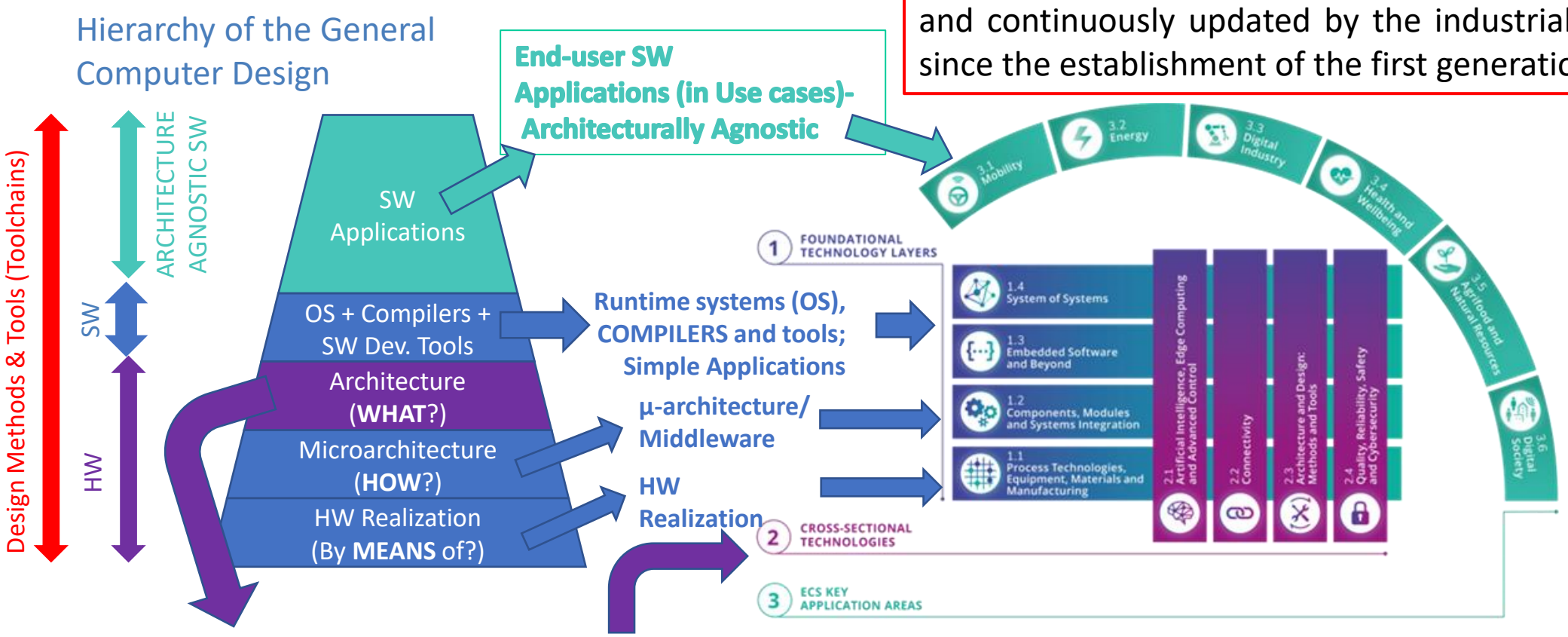
FOCUS ON RISC V - CHIPS JU'S GUIDING PRINCIPLES

- The EC, in cooperation with KDT/Chips JU, has set-up Working Groups of experts from prominent European Industrial and Academic leaders.
- These Working Groups propose RISC V R&D&I (general or specialized) roadmaps.
- The Governing Board of Chips JU critically reviews these roadmaps and incorporates them into the Multiannual Work Programme:
  - **Bottom-up:** updates of SRIA to compete with all other ECS proposals.
  - **Top-down:** focused thematic calls for proposals.
- Key guiding principles applied by Chips JU over the RISC V activities:
  - Assume a holistic, architecture-centric approach: ***HW/SW IPs*** + ***EDA*** Tools + ***SW Development*** Tools.
  - Ensure compatibility with the RISC V architecture (ISA, registers, programming models).
  - Build on existing assets in EU (IPs & Tools & Apps)
  - Focus on gaps and needs, identified by industry.
  - Encourage complementarity and healthy competition among different solutions for IPs and Tools –> options & alternatives to choose from.
  - Allow smart interoperability between open-source and proprietary IPs & Tools.
  - Promote successful open-source business models (e.g., business in services, specialisations, optimisations).
  - Target industry-grade RISC V developments to diversify existing architectural solutions.

How does Computer Design Fit in the ECS-SRIA?

The Bottom-Up Approach

ECS SRIA – a **multiannual strategic document**, created and continuously updated by the industrial associations since the establishment of the first generation JUs.



Since 2023, **SRIA** has been **extended with RISC V** content

ARCHITECTURES + EDA Tool chains + middleware, system SW, drivers

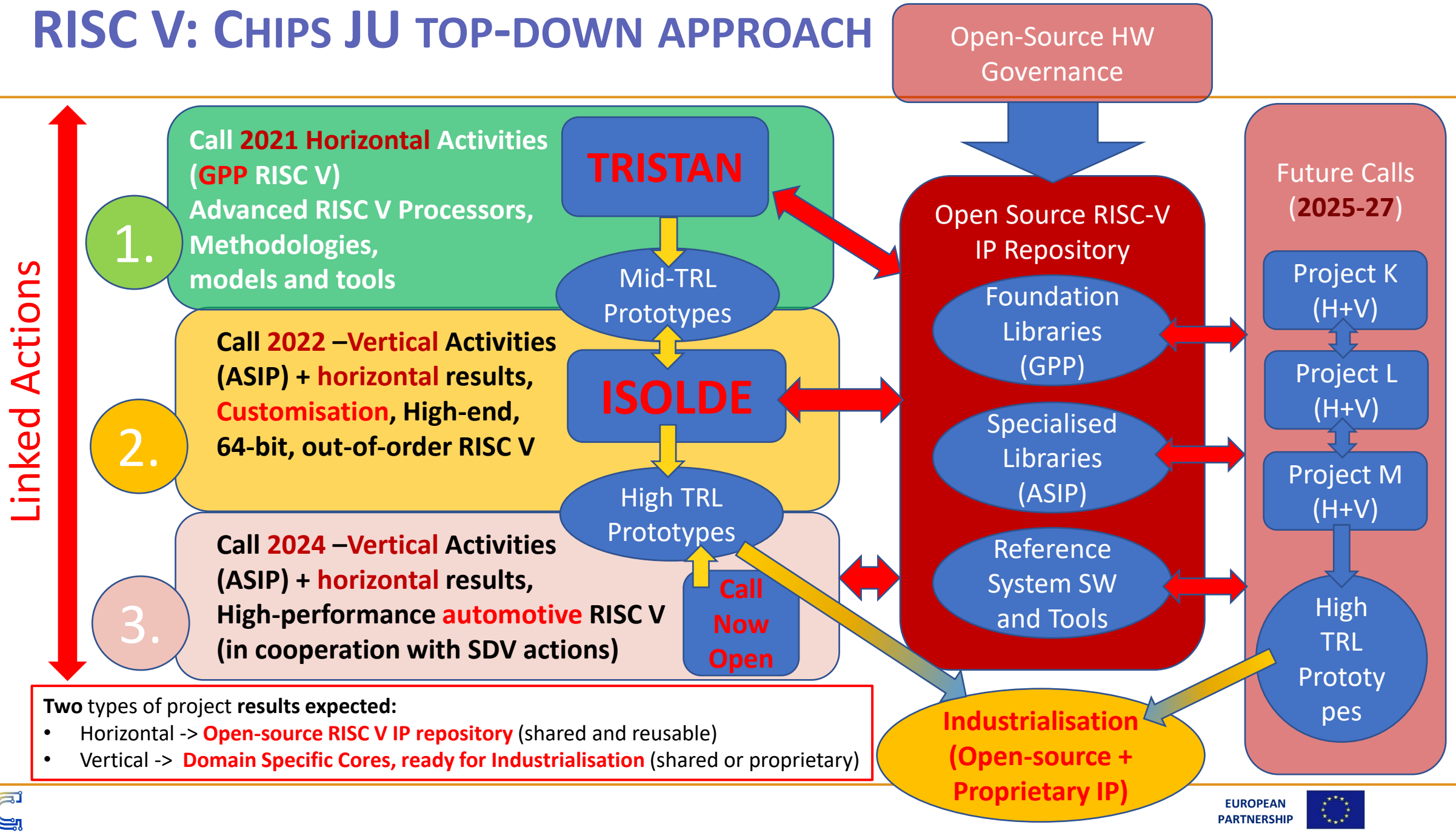
Various RISC V developments have been accomplished within ECSEL JU and non-initiative Chips JU projects

CHIPS JU FOCUS TOPICS
TOP-DOWN PROGRAMME STEERING

- **Focus topics in general:**
  - **Complement** the "bottom-up" **SRIA**
  - Initiated by the Chips JU's stakeholders: **private members (3IA)**, **Participating States** or the **European Commission**
  - Address **strategically** important areas for Europe
  - Based on **roadmaps**, prepared by WG of prominent industrial and academic leaders

- **RISC V** multiannual **focus topics:**
  - **Call 2021-IA – Focus Topic 1: Development of open-sources RISC-V building blocks – one grant awarded – TRISTAN project**
  - **Call 2022-IA – Focus Topic 3: Design of Customisable and Domain Specific Open-source RISC-V Processors – one grant awarded – ISOLDE project**
  - **Call 2024-IA – Focus Topic 2: High Performance RISC-V Automotive Processors supporting SDV – proposals under evaluation**

RISC V: CHIPS JU TOP-DOWN APPROACH



Two types of project **results expected:**

- Horizontal -> **Open-source RISC V IP repository** (shared and reusable)
- Vertical -> **Domain Specific Cores, ready for Industrialisation** (shared or proprietary)

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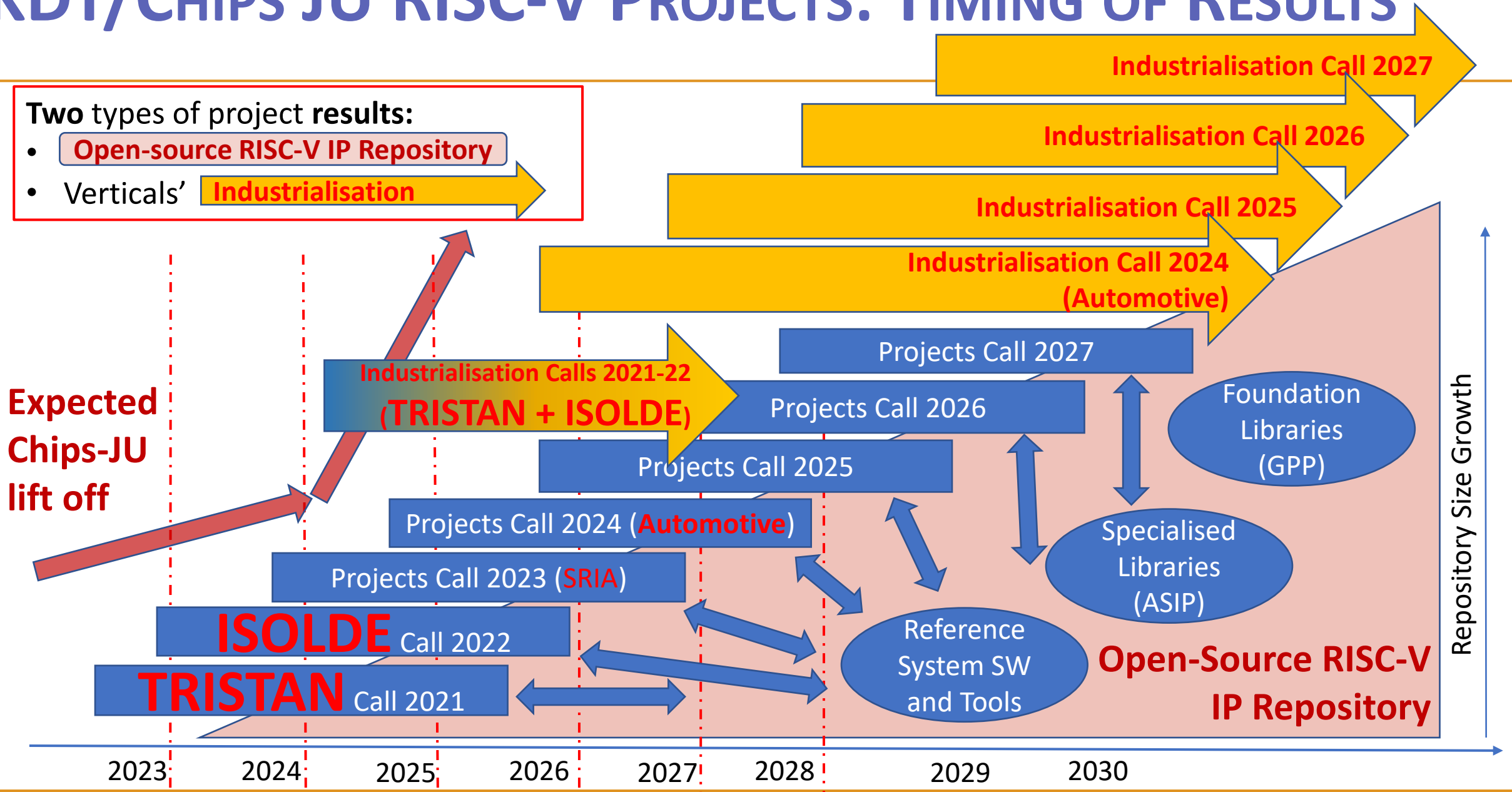
KDT/Chips JU RISC-V Projects: Timing of Results



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RISC V AND CHIPS JU AT A GLANCE

Prior work

- **ECSEL heritage** - The ECSEL portfolio covers a variety of RISC V aspects at a **project task level**
  - **Scope: architecture** extensions (e.g., accelerators, co-processors); (Low Power/High Performance) **microarchitectures** (e.g., implementations of the architectures);(Low Power) HW **realizations** (e.g., FDSOI – By MEANS of?); **SW support** for RISC V: System SW and tools for design, verification, testing, etc.
  - **ECSEL projects with RISC V** tasks - **OCEAN 12 (2017-1-IA), CPS4EU (2018-1-IA), VALU3S (2019-2-RIA), FRACTAL (2019-2-SP2), Energy ECS (2020-1-IA), StorAIge (2020-1-IA), DAIS (2020-2-RIA) – most of these have also addressed AI.**

Strategy building

- **KDT JU/Chips JU RISC V strategy – focused and linked actions**
  - Recommendations and **Roadmap for European Sovereignty** in Open Source Hardware, Software, and RISC-V Technologies , 2022
  - **SRIA update on RISC V, 2022**
  - **Automotive RISC V roadmap** - The Road towards a High-Performance Automotive RISC-V Reference Platform , 2023, updated 2024

Strategy Implementation

- **KDT JU/Chips JU RISC V calls**
- **Call 2021-1-IA-Focus-Topic-1-Development of open sources RISC-V building blocks**
  - **Project TRISTAN, 47 Partners,** *Total cost: € 54,371,711.93; Max HE Funding €15,597,798.00; National Funding: €13,603,678.17*
- **Call 2022-1-IA Topic 3: Focus topic on Design of Customisable and Domain Specific Open-source RISC-V Processors (IA)**
  - **Project ISOLDE, 39 Partners,** *Total cost:* € 39,410,109.71*; Max HE Funding* €11,582,733.37*; National Funding:* € 11.451.467,64

Chips JU investment in RISC V so far (2 projects contracted):
Total Cost: ***€ 95M***, HE Funding: ***€ 27M***, National Funding: ***€ 25M***, Private in-kind: ***€ 43M***

- **Call 2024-1-IA Topic 2: Focus topic on High Performance RISC-V Automotive Processors supporting the vehicle of the future**
  - **Proposals evaluation:** *Max 70 partners, Approx. cost:* ***€ 60-80M****; Max HE Funding* ***€ 20M****; Max National Funding:* ***€ 20M***

Remaining Challenges

A non-exhaustive list

Challenge 1. **Tool support** at HW and SW design levels – EDA tools but also Compilers.

Challenge 2. **System level HW design** support – families of RISC V compatible components, accelerators, peripherals, networks, memory systems.

Challenge 3. **System level SW** support – (RT)OS and middleware.

Challenge 4. **Silicon realisations**: Tape-outs, chiplets, but also PDKs for new technologies.

Challenge 5. EU industry recognize and take up RISC V to **economy-significant scale**?

Synergies with Other Activities

Leveraging success

Driven by Chips JU:

- Focus topics on **Software Defined Vehicle** (Chips JU Calls 2023 and 2024) – help in gaining industrial relevance and scale (Challenge 5).
- Focus topics on **Edge AI** systems – RISC V based solutions (Challenge 5).
- General bottom-up calls supporting the **SRIA** – e.g., medical, networking, safety critical applications and CPS design (Challenge 5), process technologies (Challenge 4), etc..
- **Design Platform Initiative** – provide tools and toolchains for holistic RISC V chip designs (mainly Challenges 1 and 4, but also 2 and 3 indirectly).
- **Pilot Lines Initiatives** – cutting edge technologies for next generations of chips – platforms for RISC V silicon realisations (Challenge 4).

Other EU funded partnerships:

- **EuroHPC** – High-end RISC V for supercomputing applications – **architectural overlaps** with high-end RISC V for CPS exist =>
  - potentials for **IP reuse** via shared libraries or repositories;
  - **common design tools** may be used after adjustments.

CONCLUSIONS

- **Chips JU's ambition** is to be a **key driver at the political level** to establish RISC V as ECS's industry standard in the EU.
- There has been an **excellent base of prior RISC V developments** and design skills established in Europe by the preceding ECSEL JU.
- **Chips-JU's top-down** and **bottom-up** approaches work together to support **linked actions at all levels** of the RISC V **design stack**– system integration, architecture, microarchitecture, tape-outs but also SW and tools.
- **Synergies** with other EU programmes can leverage success.
- **Chips JU vision –** support the development of **balanced portfolio** of RISC V families and a widely accessible IP repository, covering the entire **value and supply chains** for **thriving European industry** and **sovereignty**.

Q&A

Thank You